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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,061	09/29/2000	James J. Delmonico	1	1686

22046 7590 04/30/2004

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	11

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,061	DELMONICO, JAMES J.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28,30-32,34 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28,30-32,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 10th of March 2004 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/677,061, which the request is acceptable and an RCE has been established. Claims 18 and 30-32 have been amended; claims 9, 29 and 33 have been canceled; and claims 34 and 35 have been newly added since the Office Action was mailed on 8th of December 2003. Currently, claims 28, 30-32, 34 and 35 are pending in this application.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour [US 6,202,115 B1] in view of Barenys et al. [US 6,145,036 A; hereinafter Barenys] and Marshall et al. [US 5,915,082 A; hereinafter Marshall].

Referring to claim 28, Khosrowpour discloses a system (i.e., fault tolerant redundant bus bridge system in Fig. 1) comprising: at least one host bus master (e.g., Hub 201 of Fig. 2) operable to utilize a first communications protocol (i.e., FC Bus Protocol in Fig. 1) for communicating over a parent bus (i.e., FC Bus 202 of Fig. 2); and at least two bridge devices (i.e., First Bus Bridge 110 and Second Bus Bridge 120 in Fig. 1); said at least two bridge devices being coupled to said parent bus and a child bus (i.e., being coupled to FC Bus 202 and SCSI bus 203 in Fig. 2), said at least two bridge devices being operable to transmit messages between said host bus master and target devices (i.e., transmitting between Hub 201 and Disk Array 204 of Fig. 2; See col. 4, lines 30-41), each of said at least two bridge devices being partnered to the other bridge device (See col. 4, lines 14-27; i.e., in fact two bridges 110 and 120 are partnered via the third bus 130 in Fig. 1), said host bus master (i.e., Hub 201 of Fig. 2) being operable to use said at least two bridge devices to determine if transactions through a particular bridge are corrupted

(i.e., comparison 315, block 325 in Fig. 3 and See col. 6, lines 34-39), said host bus master being operable to verify integrity of data received from said target devices (See col. 2, lines 35-50; i.e., wherein in fact that the first and second bus bridges may comprise respective first and second RAID controllers which are operative to communicate information from a host device connected to the first bus to a mass storage element connected to the second bus in a manner appropriate to implement one or more RAID levels, the status of the first bus bridge may be communicated from the first bus bridge to the second bus bridge over a fourth bus connecting the first and second bus bridges, and an active/active failover capability may be provided implies that a host bus master being operable to use said at least two bridge devices to verify integrity (i.e., status communication for failover capability) of data received from a target devices (i.e., mass storage element)).

Khosrowpour does not teach said two bridges are LIP bridges, each LIP bridge device includes a first transceiver coupled to said host bus master over said parent bus, said host bus master utilizing said first communications protocol; a second transceiver coupled to said target devices over said child bus, said target devices utilizing a second communications protocol, said first communications protocol having a bridge device address field for addressing said bridge devices and a target device address field for addressing said target devices coupled to said child bus.

Barenys discloses I^2C expansion apparatus 200 in Fig. 2, wherein a LIP bridge device (i.e., Expansion Processor 202 of Fig. 2) including, a first transceiver coupled to a host bus master (i.e., communication means of bus master on primary bus) over a parent bus (i.e., a primary bus; in fact, a first transceiver coupled to said host bus master for I^2C transaction; See col. 3, lines 22-29), said host bus master utilizing said first communications protocol (i.e., extended I^2C protocol for the communication between primary bus master and sub-bus slave via expansion processor, such that Primary Bus Transfer Sequence 301 of Fig. 3A and 3B; See col. 5, line 60 through col. 7, line 17); a second transceiver coupled to target devices (i.e., communication means of said expansion devices on sub-bus) over a child bus (i.e., sub-bus 232 of

Fig. 2), said target devices utilizing a second communications protocol (i.e., a standard I^2C protocol; See col. 5, lines 8-26), said first communications protocol having a bridge device address field (i.e., expansion processor address field 304 of Fig. 3A) for addressing said bridge devices (See col. 6, lines 7-9) and a target device address field (i.e., sub-bus code 307 and expansion device address 309 in Fig. 2, as combined) for addressing said target devices coupled to said child bus (See col. 6, lines 22-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said bridge devices with their buses, as disclosed by Khosrowpour, by said LIP bridge devices with their buses, as disclosed by Barenys, for the advantage of providing an advantage of a fault isolation, thereby a failing device on one of said target devices (i.e., the components on secondary busses) would not cause a failure on the entire parent bus (i.e., primary I^2C system bus), which is disclosed by Barenys at col. 1, line 62 through col. 2, line 8.

Khosrowpour, as modified by Barenys, does not teach said host bus master being operable to cross check data provided by each of said at least two LIP bridge devices to verify said integrity of data, and each of said at least two LIP bridge devices being adapted to use partnering signals to reset the other LIP bridge device to isolate faults.

Marshall discloses an isolation logic 62 (Fig. 8) for an error and fault isolation (See Fig. 7), wherein a host bus master being operable to cross check data (i.e., independently generated results being compared in order to detect an error originating in one processor) provided by each of at least two LIP bridge devices (i.e., each of Master Processor and Slave Processor in Fig. 7) to verify integrity of data (See col. 1, lines 13-21), and each of said at least two LIP bridge devices being adapted to use partnering signals (e.g., Lockstep Disable, Processor 1 Disable, Memory Address Error, etc. in Fig. 7) to reset the other LIP bridge device (See col. 9, lines 1-4; i.e., wherein in fact that the slave processor disables the master processor and makes the slave processor the active processor implies that partnering signal to reset (i.e.,

change the active processor from the master processor to the slave processor) the other bridge device (i.e., master processor)) to isolate faults (See col. 2, lines 7-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said isolation logic, as disclosed by Marshall, in each of said at least two LIP bridge devices, as disclosed by Khosrowpour, as modified by Barenys, so as both of said at least two LIP bridge devices (i.e., master processors and slave processor) to analyze an error to isolates the faults (i.e., failure) and to determine what corrective action is to be taken (See Marshall, col. 5, lines 15-17).

Referring to claim 30, Khosrowpour teaches said host bus master (i.e., Hub 201 of Fig. 2) is operable to hold a failed interconnected LIP bridge device (e.g., PCI-PCI Bridge 214 of First Circuit Assembly 205 in Fig. 2) in a reset state (i.e., failed state) in which said failed interconnected LIP bridge device (i.e., PCI-PCI Bridge of First Circuit Assembly) is electrically removed from said child bus (i.e., SCSI bus 203 in Fig. 2; See col. 6, lines 44-46; i.e., wherein in fact that information addressed to the first bus bridge may be routed through the second bus bridge until the first bus bridge is available implies that said failed interconnected LIP bridge device is electrically removed from said child bus).

4. Claims 31, 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour [US 6,202,115 B1] in view of Barenys [US 6,145,036 A] and Marshall [US 5,915,082 A] as applied to claims 28 and 30 above, and further in view of Staab [US 4,377,000].

Referring to claim 31, Khosrowpour, as modified by Barenys and Marshall, discloses all the limitations of the claim 31 except that does not expressly teach said host bus master clears errors in said failed interconnected LIP bridge device with reset commands.

Staab discloses an automatic fault detection and recovery system (See Abstract), wherein a host bus master (i.e., device handler) clears errors in a failed interconnected LIP bridge device (i.e., peripheral device) with reset commands (See col. 5, lines 19-22 and 38-41).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said device handler (i.e., LIP bridge device handler), as disclosed by Staab, in each of said host bus master, as disclosed by Khosrowpour, as modified by Barenys and Marshall, for the advantage of providing for safe and reliable automatic recovery and compensation for said faults (i.e., failure), which is disclosed by Staab, at col. 2, lines 39-42.

Referring to claim 32, Khosrowpour teaches said host bus master (i.e., Hub 201 of Fig. 2) is operable to access any target device (e.g., Disk Array 204 in Fig. 2) on said child bus (i.e., SCSI bus 203 of Fig. 2) via any LIP bridge device (i.e., any PCI-PCI Bridge 214 or 244 in Fig. 2) connected to said parent bus and said child bus (i.e., FC bus 202 and SCSI bus 203 in Fig. 2; See col. 4, lines 54+).

Referring to claim 34, Marshall teaches said host bus master (i.e., Receiving Function 20 of Fig. 2) performs every child bus read operation on said at least two LIP bridge devices (i.e., Master Processor and Slave Processor in Fig. 7) to ensure data integrity (See col. 1, lines 13-21; i.e., wherein in fact that the same task with master and slave processors' independently generated results being compared in order to detect an error originating in one processor implies that performing every child bus read operation on said at least two LIP bridge devices (i.e., comparing results of the same task) to ensure data integrity).

Referring to claim 35, Marshall teaches each of said at least two LIP bridge devices (i.e., each of Master Processor and Slave Processor in Fig. 7) are adapted to use partnering signals (e.g., Lockstep Disable, Processor 1 Disable, Memory Address Error, etc. in Fig. 7) to disable the other LIP bridge device (See col. 9, lines 1-4; i.e., wherein in fact that the slave processor disables the master processor and makes the slave processor the active processor implies that partnering signal to disable the other bridge device (i.e., disable the master processor)) to isolate faults (See col. 2, lines 7-10).

Response to Arguments

5. Applicant's arguments with respect to claim 28 have been considered but are moot in view of the new ground(s) of rejection.

In fact, in response to the Applicant's arguments with respect to Barenys does not specifically disclose two expansion processors interconnected on a parent bus, in the claim 28, the Examiner brought Khosrowpour as a primary reference, which suggests two bridge devices interconnected on a parent bus, and Barenys teaches LIP bridge device as a secondary reference. Thus, the combination of Khosrowpour and Barenys with rationale obviously suggests the claimed subject matter "at least two LIP bridge devices".

Furthermore, in response to the Applicant's arguments with respect to (1) Khosrowpour does not teach that the host master is operable to cross check data provided by each of said at least two LIP bridge devices to verify integrity of data received from said target devices, and (2) Khosrowpour does not teach each of said at least two LIP bridge devices being adapted to use partnering signals to reset the other LIP bridge device to isolate faults, in the claim 28, the Examiner brought Marshall reference in the rejection for the limitations which are not provided by Khosrowpour and Barenys.

See the paragraph 3 of the instant Office Action, Claims 28 and 30 rejection under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour in view of Barenys and Marshall.

Therefore, the Applicant's arguments on this point are not persuasive.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gulick et al. [US 6,618,782 B1] disclose computer interconnection bus link layer.

Stancil [US 5,897,663 A] discloses host I^2C controller for selectively executing current address reads to I^2C EEPROMs.

Schutte [US 6,038,623 A] discloses electronic network allowing multi-speed communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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